FemtoFarad/TeraOhm Endpoint Detection for Microsurgery of Integrated Circuit Devices

Jim Colvin
36217 Worthing Dr., Newark, CA 94560 USA

Abstract

Interactive electrical endpoint detection when thinning conductive and capacitive materials opens the door to approaching a suspect site in an IC without relying on the traditional iterative approach. Controlled approach of embedded conductors in insulators (packages) as well as controlled die thinning with submicron control will be shown, allowing safe approach to the desired feature without overshoot.

Introduction

Creating access points in an IC has traditionally required iterative guesswork to reach the target. Laser decapsulation places the surface at risk due to ablation damage caused by the glass beads. Non-uniformity of removal is problematic both chemically and with the laser. This paper will demonstrate a novel endpointing technique with, currently, <1µm control using capacitive detection through the package or insulator. Thinning with a resolution below 1 micron enables controlled and repeatable removal of material, obviating the need to "stop and look"[1,2]. Embedded defects can now be quickly approached both horizontally and vertically, greatly reducing the chance of overshoot by monitoring during the removal, the local capacitance and resistance as the insulator is thinned. Masking methods to expose multiple areas will be discussed along with local Capacitive/Resistive mapping of embedded features. Resolution improvements using guard ring technology is anticipated to improve resolution to <40nm for electrostatic detection. Resistive detection is limited by tip geometry.

Background

Experimental setup:
A modified UltraTec ASAP-1 IPS digital polisher along with an electrically isolated mount plate, shown in figure 1, was used[3].

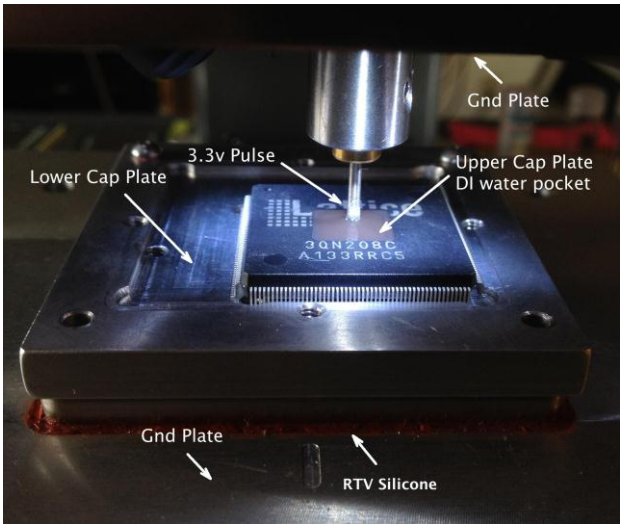


Figure 1: Image of 208 PQFP mounted to test plate with crystalbond wax. At least one of the leads needs to be in contact with the mounting plate to the die. Note: the water stays in the cavity due to surface tension, defining the upper plate of the capacitor.

Figure 2 is a basic circuit diagram of the endpoint detector system. Since requirements are to sense capacitively down to 10 fF and resistively up to 1 TΩ. A high impedance instrumentation amplifier was used at the front end of the detection circuitry to monitor voltage swing on the mounting plate. Capacitance of the plate was increased from 20 pF to 100 pF based on current experimental results, but is adjustable to suit the need by adding external capacitors (C1). The charge on the plate can drift with capacitance so it is necessary to add approximately 1 TΩ of resistance (Bias at R2) tied to the midpoint voltage to control drift.

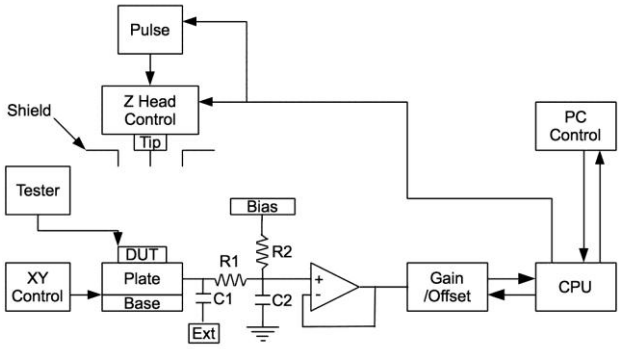
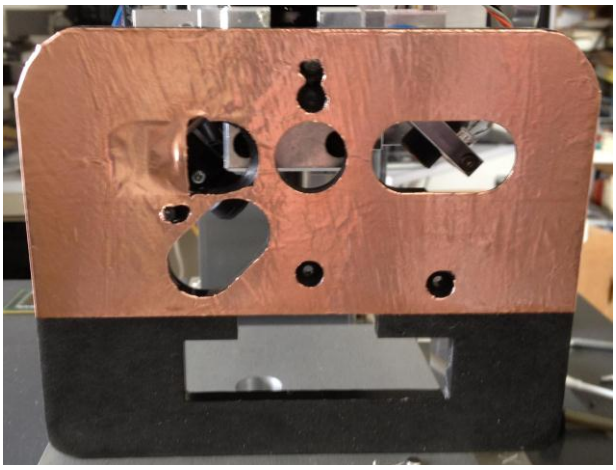


Figure 2: Circuit diagram of endpoint detector.

The upper and lower main plates were tied to ground to minimize interference and parasitic capacitive influence caused by head height changes. The milling spindle was configured to drive a coupled 3.3V pulse signal to the milling/polishing tip. See figure 3. The mount plate was isolated above the lower ground plate and tied to the input of an instrumentation amplifier.



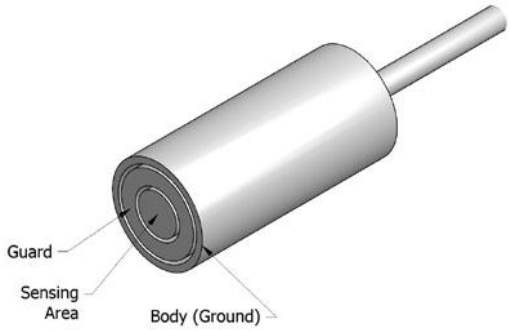


Figure 3: Copper tape is added to form a ground shield around the milling spindle. This reduces AC interference and crosstalk capacitance. Tip electrostatic field focusing can be improved with guard technology around the milling spindle tip when used as a sensor. This is anticipated to improve sensitivity to <40nm and allow improved local mapping. Commercially available sensors are reported to measure better than 12nm.[4,5]

Software/hardware was modified to do the following:

1. Differentially detect the capacitively coupled charge transferred to the mount plate from the spindle tip into the low fF range and high GΩ range.
2. Sample and remove local AC interference.
3. Accumulate and average the data stream, displaying a running result during operation, and control DC drift in purely capacitive environments.
4. Provide force feedback control and closed loop operation of the capacitive endpoint to auto stop at a predetermined value.

Since distance is inversely proportional to capacitance for a parallel plate capacitor, equation 1, the endpoint reading accuracy drastically improves as the target endpoint is approached. A capacitive response yields a square wave based on the ratio of charge transferred to the lower sensor plate per equation 2 [6,7]. The pulse rate is differential at ¼ line frequency =7.5 Hz. A resistive component will show as an RC time constant based on time to charge the 100 pF plate through the resistor, similar to figure 4. The software samples and discriminates capacitance (slope = 0) from resistance. Since DI water has resistivities of 20 MΩ-cm or less it will appear as a short circuit in endpoint[8]. Mineral oil and crystal bond wax (hot wax) are covalent and therefore non-conductive. Both can serve as masking materials for exposed areas, opening the door for various access techniques.

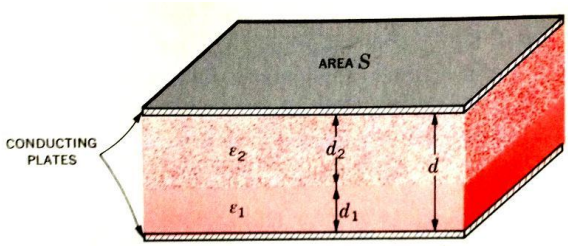
Any crack or breach in the insulator will show conductively, depending on the chosen fluid, providing a safe early halt to the process. A crack causing early endpoint detection can be masked with mineral oil or crystalbond, then DI or distilled water reapplied to continue the process until reaching bonds or any other desired endpoint.

$C = \varepsilon * E_o * A/D$, where $E_o = 8.854 \times 10^{-12}$ (Equation 1)

ε = dielectric constant of the material
A = overlapping surface area of the plates
D = distance between the plates
C = capacitance

Or for 2 differing dielectric materials:

$$C = 1/[(d_1/\epsilon_1 S) + (d_2/\epsilon_2 S)]$$



$i = C\, dv/dt$ (Equation 2)

Resistive Endpoint Detection:
The part is attached to the plate using hot wax with one or more leads in contact to form the lower plate. The desired area to open and tool are selected or loaded from a previous recipe. Tilt is corrected, and then a preliminary pocket 100µm deep is cut. The surface is wiped clean and DI water is added only in the pocket. Surface tension holds the water in the pocket; however, it is of little concern since capacitance values are secondary for this example. The milling process proceeds until the

endpoint jumps with a reduced resistance value due to bond wire contact with the DI water, typically through a local crack or pocket in the plastic proximal to a bond wire, typically a few minute operation. Figures 5, 6 and 7 show the result.

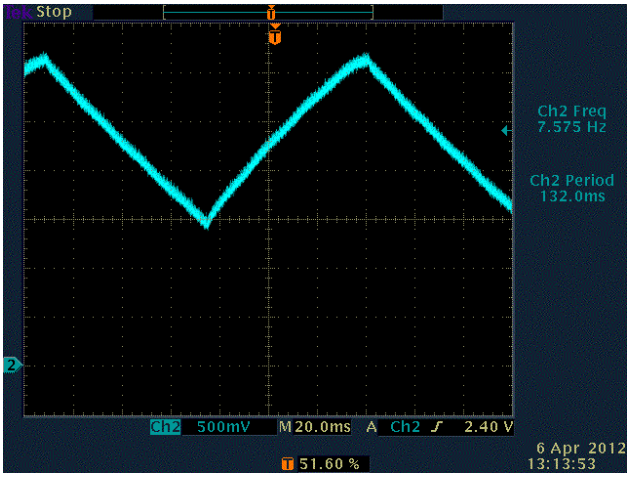


Figure 4: Measured leakage from back to back 1n914 signal diodes on the order of 200 MΩ. Plate capacitance =100 pF. A design criterion is to make I_o leakage measure as a strong detected endpoint signal.

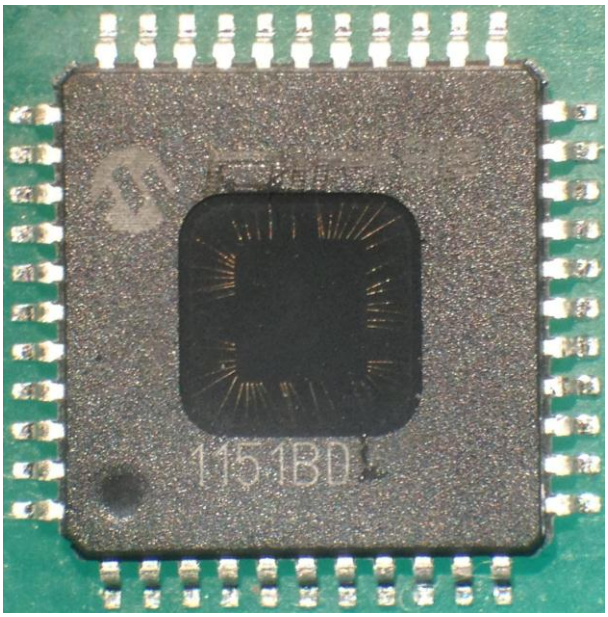


Figure 5: Note visible wire loops embedded in the remaining thin plastic layer. DI water enhances the image contrast. Crystalbond wax can be used for capacitive endpoint thinning inside the wire loops, leaving 10µm or more of remaining plastic over the die, if desired.

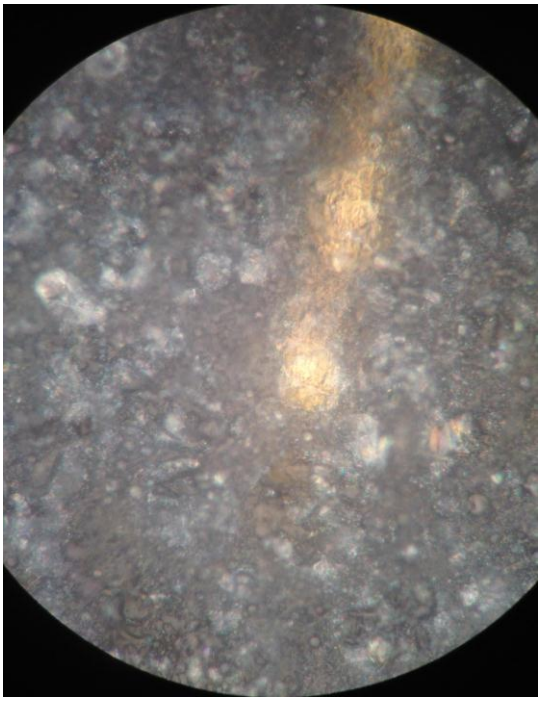


Figure 6: 100X objective used to image wire prior to crystal bond application, confirming wires are still embedded in plastic. Remaining thickness = 5um.

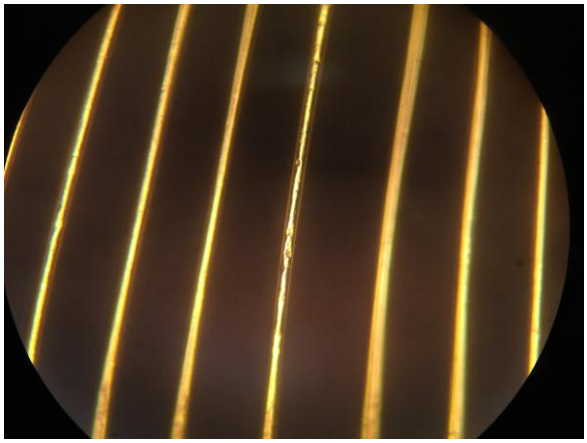


Figure 7: 20X objective used to image wire tops after chemical removal of epoxy. Resistive endpoint signal reaches saturation with <5µm remaining plastic. Only minor impact damage of the wire top is seen from the glass frit.

Masking the Resistive Endpoint:
If an endpoint is obtained due to an unwanted area, such as a lead finger, crack or exceptionally high wire loop, being exposed, the pocket can be rinsed out, dried and coated with a thin layer of mineral oil to isolate the endpoint signal. The area is retargeted and DI water added. The disturbed areas from milling will wet with all other areas remaining isolated. Endpoint will occur on approach of next feature related to milling area.

Capacitive Endpoint:
Similar to the resistive methods described above, the part is mounted and the cavity outline defined. The cavity over the die inside the bond loops can be cut first or masked and cut last. The advantage to the latter, is the ability to verify lead dress location if x-ray imaging is not available, fill in the pocket with hot wax and mill the wax for the interior pocket. Fluid tension will keep the DI water in the pocket for either method. Mineral oil should not be used since the wall cannot be rebuilt to the surface of the part. The water must be contained in a constant area.

Milling proceeds while monitoring the endpoint. The area of the floor cut by the milling tool, not the tool diameter, determines the capacitance. As the floor descends, the capacitance increases proportionately to the decreasing distance. Figures 8 and 9 show the increase in capacitance as the die is approached. As the slope of capacitance increases, the z increment is reduced. For this device, 25µm, then 10µm then 1µm increments were used, with recorded measurements taken every 5µm. Obviously aggressive removal can be done until the last 100 to 200 µm from the target to save time. Endpoint based on prior experience can be done in 5 to 10 minutes depending on area and tool size used. Unknowns (no x-ray or practice part) can take 30 minutes or more with caution exercised. Figure 10 shows the finished part. The interior cavity is 30µm deep, the interior cavity is over the lead dress, resistively end pointed, and the outer 2 cavities are 500µm and 1000µm deep, respectively, allowing microscope objective clearance. Figures 11-12 detail the remaining plastic in the pocket over the die. This part is ready for analysis and/or final decap to remove the thin remaining layer. A BSETEQ PLASER inductively coupled plasma was used to decap the remaining plastic over the die, as shown in Figure 13[9].

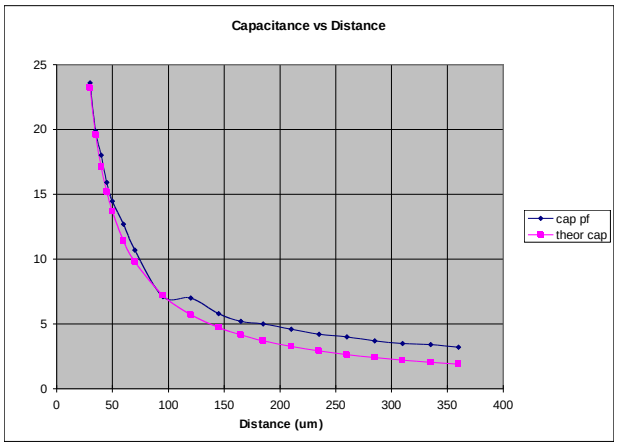


Figure 8: Graph of capacitance during milling. The jump from 120µm to 360µm is due to liquid sitting over the cavity edge creating error with increased plate area for the capacitor.

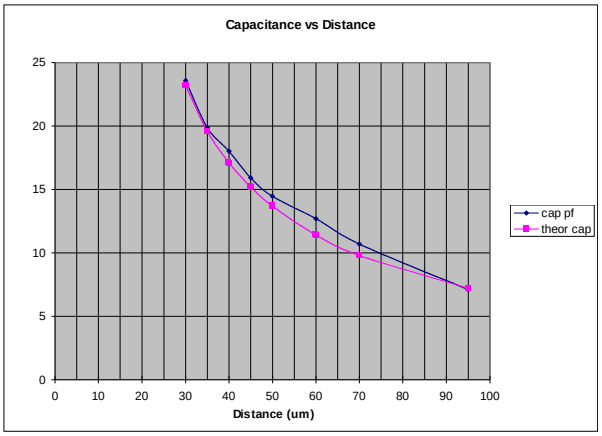


Figure 9: Expanded graph of capacitance during milling. Worst-case error is 5µm at 60µm remaining thickness. Amplifier drift issues were found and corrected.

Figure 10: Step milling operation to endpoint resistively above the wire loops and capacitively over the die surface. No masking needed since the interior pocket was milled first. Target= 30µm +-1µm for the die and 5-10µm above the wire loops.

No Laser decap methods were used since the surface was alternatively thinned using the capacitive endpoint method. Note the innermost cavity is now removed, exposing the die surface. Laser decap leaves too much material to be quickly removed by dry etch methods and risks the die since the glass frit can act as a lens, locally focusing the laser energy on the active die surface. All devices were test verified after prep to confirm functionality.

Figure 11: Optical verification after endpoint. Note the orange color in the bottom cavity reflected from the die.

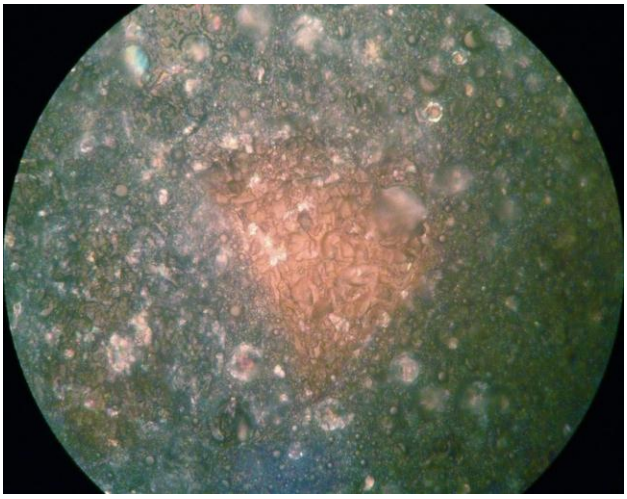


Figure 12: 100X objective view of the bottom cavity with view of light scattering up through ground glass particles at 30µm remaining package thickness.

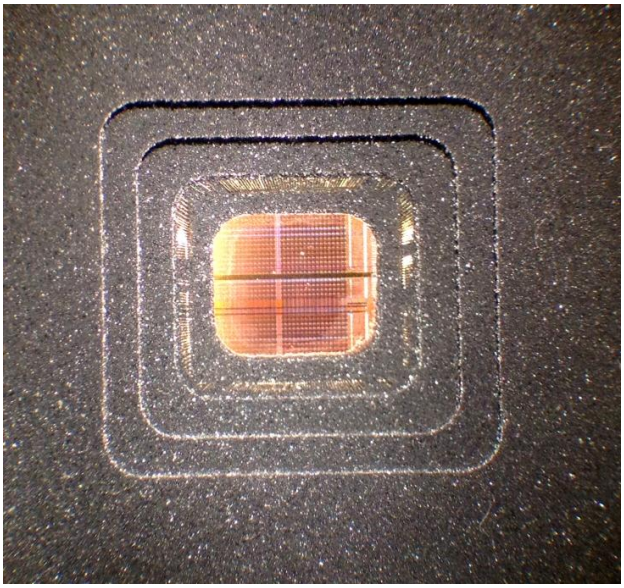


Figure 13: Plasma decap of package from figure 10. Decap accomplished using a BSETEQ PLASER decap system. Total time to clear innermost cavity was 25 minutes using a $CF_4/0_2$ then a dedicated O_2 plasma fillerblast process to finish. Etch power used was 30 watts.

Locating a resistive leakage zone:
If an endpoint read has occurred, close inspection may not reveal the local region responsible. If the location needs to be identified, such as a suspected crack, a bead of water is suspended from the tip and the tip is moved slowly over the cavity hovering above the surface. A positive reading shows the proximity of the leakage. The water trail evaporates behind the tip allowing the area to be triangulated. This method was used to identify the highest exposed bond wire in figure 7. Local passivation removal with endpoint using colloidal silica or other ionic polishing compounds is accomplished using the same principles outlined above.

Potential Issues:

1. Dry milling resistive endpoint requires the tool to physically contact the wire resulting in excessive damage. Additionally tribo-charging of the material during removal causes wild DC swings on the endpoint. Use DI or similar solution.
2. False early endpoint can occur if package leads or surface caps couple to the cavity due to residue or splashing. Masking methods can be used if needed.
3. Die tilt needs to be checked on approach at around 60µm and corrected using tip scan methods to map the local capacitance variation over the die.
4. Capacitance data can be erroneous due to die coat, tilt or delamination issues. A resistive endpoint is typical for delamination or cracks to

prevent die damage since the liquid will enter and wet a bond underneath.

5. Lateral parasitic capacitance was largely ignored, as was the issue of varying dielectric constants in the material. Special cases may require characterization. Generally the parasitic from the lead dress and lead frame can be ignored since the primary signal will dominate on approach to endpoint.

Resistive Endpoint Thinning of Silicon

The resistive endpoint method can be used to thin silicon substrates on a variety of packages. The setup differs since polarity now matters and the substrate leakages will be well below the GΩ range, actually into the 100kΩ range or less for tip scan measurements. Several modifications and observations for the setup are required:

1. Capacitance plate measurement method will not work in most cases due to the conductive nature of the substrate.
2. Resistive substrate method covering the pocket area using an ionic liquid will result in low impedance readings making local thinning 2D readings problematic. The tip will need to be locally conductive (tip core insert or tip containing one or more soft alloys of Cu, Al, C, Pb, Sn, Sb, Au, In) and covalent compounds will need to be used, such as oil.
3. Need to sweep through positive and negative measurements to determine the IV curve and resulting breakdown. Resistance alone can be used but threshold is independent of resistance so it represents the best metric for thickness.
4. Conductive tip design and interface becomes important since the tip cannot rely on the fluid to provide conductivity but must maintain intimate contact with the silicon as it is scanned and removed.

Characterization and Calibration of Silicon Endpoint:
The part can be mounted while on the board or individually as shown in figures 14 and 15. Since we are not concerned with capacitance endpoint and the impedances are in the KΩ range the large board poses no problem. The die surface is tilt corrected and normally heated to relax the stress as described in another paper in this proceedings[10]. For this experiment, die curvature will be deliberately left in order to characterize and validate the endpoint method. The surface was polished to 50µm globally, then pocket polished further with a 2mm diameter Xylem tool with the traditional iterative method. Once an open area was observed the process was halted. Figure 16 is the result. A scan line at 0,-690 to -1000,-690 µm was chosen, based on a 0,0 origin in the center of the pocket.

Figure 14: Graphics card mounted and electrically connected to floating endpoint sensor plate.

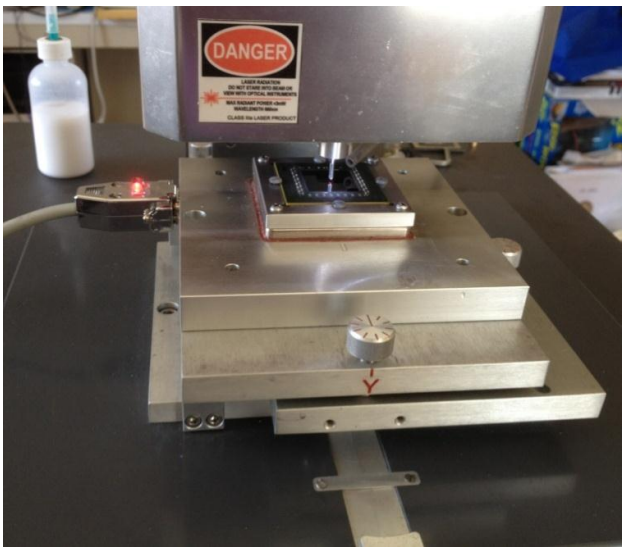


Figure 15: BGA mounted and electrically connected to the floating endpoint sensor plate. Nylon screws provide a constant gentle down pressure to hold the balls in contact with the plate.

The equation that was used to calculate the thickness variation on the parts thinned based on interference patterns is shown in Equation 3[11].

$$\Delta t = (\lambda * OPD)/(2*n) \qquad \text{(Equation 3)}$$

n = index of refraction = 3.434 for silicon
Δt = change in silicon depth.
λ = wavelength of light.
OPD = number of observed fringes.

Putting in the constants (n and λ) the equation can be simplified for silicon at 1064nm in Equation 4 below:

$$\Delta t = OPD*0.155 \qquad \text{(Equation 4)}$$

The fringes are counted to precisely represent the thickness at each coordinate allowing characterization of the relationship between threshold and thickness.

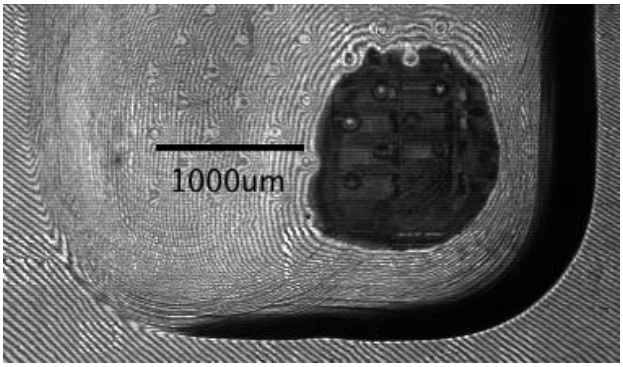


Figure 16: LSM image at 1064nm of fringes in a 4mm pocket. Scale bar is matched over region of X-axis line scan from the portion 0,-690 µm to -1000,-690 µm.

A 150µm soft carbon scan tip was used in figure 17 to profile the electrical characteristics of the substrate with a loading force of 5 grams for the general area in X and Y to identify the relationship between thickness and resistance. Note: Soft metal tips can also be used. The resulting scan line plot is shown in figure 18. Figures 19 and 20 show the shift in reverse bias substrate breakdown at 2 coordinates on each end of the scan line from x=-500 to x=-1000µm. The breakdown moves to lower voltages as the active p-n junctions are approached. Figure 21 shows the resulting curve of thickness vs. diode threshold.

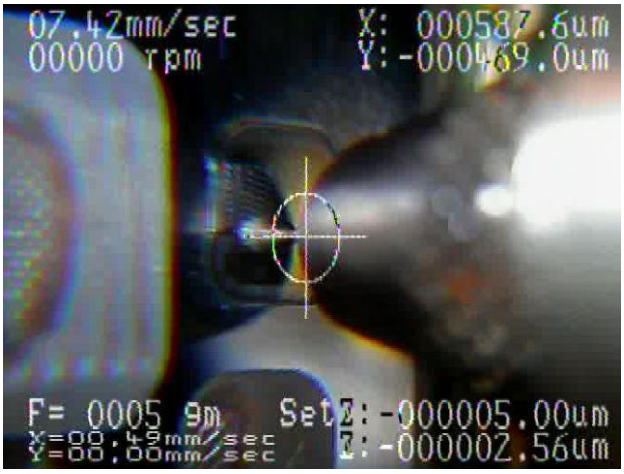


Figure 17: Soft carbon conductive tip touchdown and area scan to map remaining silicon thickness and identify minima. A 150µm scan tip was used.

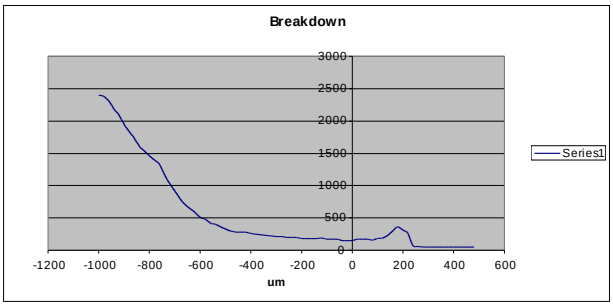


Figure 18: Plot of approximate diode threshold voltage vs. tip location for the 150µm diameter tip.

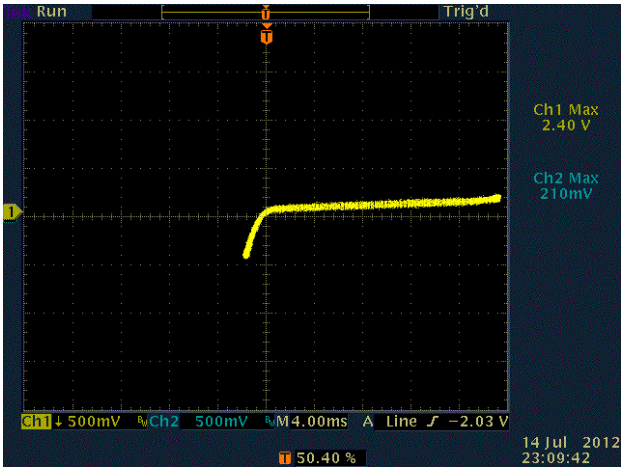


Figure 19: Resulting curve characteristic at -1000,-690 µm. Settings: 1V/div, 50ua/div. Si thickness=4.65µm

Figure 20: Resulting curve characteristic at x=-500,-690 µm. Settings: 1V/div, 50ua/div. Si thickness=2.48µm

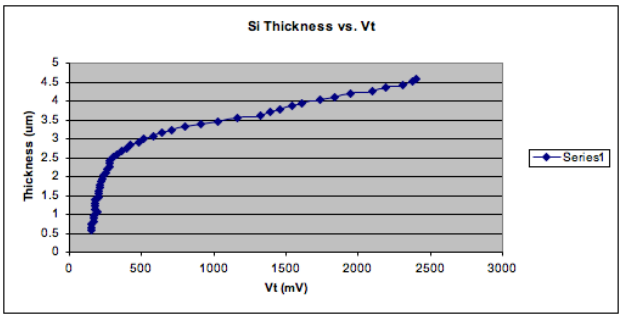


Figure 21: Plot of Si thickness vs. diode substrate threshold.

A new 4x4 pocket was thinned using a modified Xylem tip with a soft metal conductive core insert. Endpoint detection was used and the process stopped when any portion of the scan showed a moving breakdown below 3.3V. Thinning continued for a target endpoint at >2µm while parametrically monitoring the substrate. Figure 22 is the laser scan image (LSM) showing fringe minima on the lower left and the corresponding conductive scanning probe microscope image C-SPM. Tip scan conductivity using a soft 150µm carbon tip down to 2 grams constant force on the ASAP-1 IPS confirms the minima at 2.5µm of remaining silicon, correlating perfectly to the LSM image. The ridge is generated by tip convolution along the wall of the silicon.

Substrate thinning of epitaxial or degenerate substrates is accomplished with similar methods except the substrate leakage will change from low ohmic to a diode behavior as the active area below the doped substrate is exposed. Characterization is recommended on a sacrificial unit to identify the expected electrical characteristic versus thickness for a given process technology.

It should be clear from this work that the Ultra Tec ASAP-1 IPS system has been reconfigured as a scanning probe microscope (SPM) meeting the three basic definitions of an SPM[12]:

1. A scanning tip.
2. X, Y, Z dimension scan control.
3. Force feedback.

Current can be injected or an electrostatic field formed or measured from the scanning tip. Local 2D/3D capacitance/magnetic/conductive SPM mapping will be added to the software. Mapping, in combination with milling and polishing capabilities, eliminates the need to go between different tools – offering a clear step towards the universal tool that FA Engineers are keen on finding[13]. Moreover, the combination approach opens the door to in-situ characterization, including local injection of current into an active substrate for latchup or similar sensitive node localization with a scanning tip. Mapping and feedback control of local conductive, electrostatic, and magnetic fields interactive with material removal becomes possible.

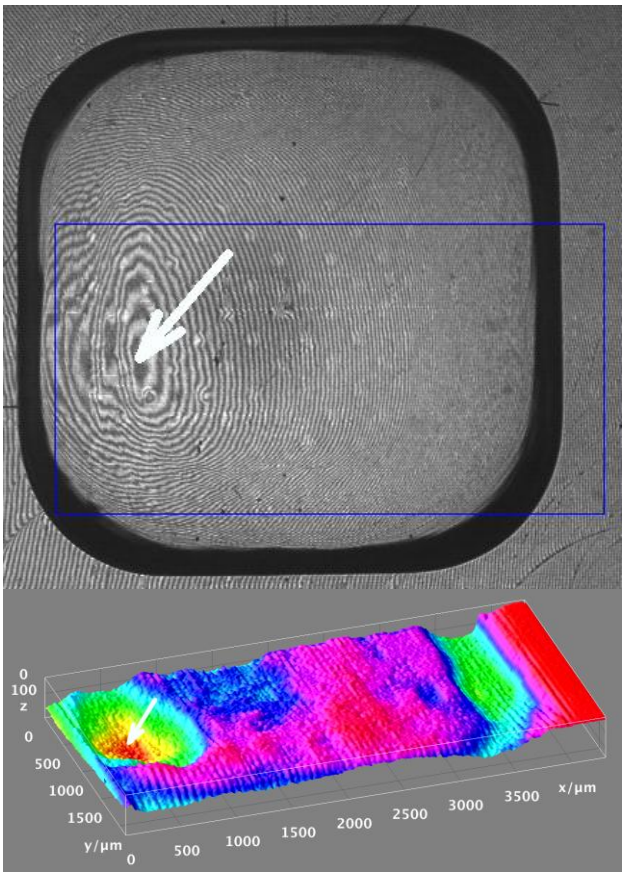


Figure 22: Another 4x4mm area thinned on a deliberate tilt to confirm endpoint capability. Spot is thinnest at 2.5µm on the left. Upper image shows the fringes at 1064nm and lower image is a C-SPM image produced on the ASAP-1 IPS machine taken in the blue boxed region. The C-SPM image corresponds to the LSM fringe bullseye pattern.

Conclusions

Controlled microsurgery has been demonstrated with capacitive and resistive feedback control. This opens the door for improved resolution with SQUID Microscopy, INSB thermography (Lock-In), Thermal Laser Stimulus and similar techniques without fully exposing the die topside or stopping at the desired critical target thickness on silicon from the backside. Multiple pockets can be created with each prior pocket masked enabling complex multiple access points to an IC or multi chip module. Dendritic leakage issues can be monitored and approached allowing the remaining 5µm to 10µm of plastic to be ion milled for surface science analyses. Plastic removal issues with copper wires, especially fine pitch wires damaged with acid and/or Laser techniques, can also be alternatively exposed using slower plasma methods due to much thinner plastic profiles. Capacitance and resistive mapping of local features by

scanning/milling with the tip opens up a world of new possibilities.

Acknowledgments

Many thanks to William Lo and Tim Hazeldine for manuscript review. I would also like to thank my wife for supporting my many hours assembling this manuscript.

References

[1] D. Scott, E. O'Donnell, T. Malik and R. Jain, "Global Die UltraThin Silicon for Backside Diagnostics and Circuit Edit," *ISTFA 2009 Proceedings,* pp. 110-118, 2009.

[2] T. Lundquist, E. Delenia, J. Harroun and E. LeRoy, "Ultra-Thinning of C4 Integrated Circuits for Backside Analysis," *Elsevier Science Ltd.,* pp. 1-5, 2001.

[3] ASAP-1 IPS Product Datasheet, Ultra Tec Mfg, Inc., Published November 2010. http://www.ultratecusa.com/asap-1-ips

[4] http://www.mtiinstruments.com/technology/ Capacitance.aspx (Capacitance probe theory/resolution)

[5]http://www.lionprecision.com/tech-library/technotes/cap-0020-sensor-theory.html

[6] William H. Hayt, Jr., "Engineering Circuit Analysis," 3rd Edition McGraw-Hill, p.146, 1971

[7] William H. Hayt, Jr., "Engineering Electromagnetics," 4th Edition McGraw-Hill, p.163, 1981.

[8] http://www.circuitnet.com/experts/59891.shtml (DI water resistivity).

[9] BSET EQ Plaser Web Datasheet, http://www.ultratecusa.com/plaser

[10] J. Colvin, H. Patel, T. Hazeldine, "Stress Reduction during Silicon Thinning Using Thermal Relaxation and 3D Curvature Correction Techniques," *ISTFA 2012 Proceedings,* 2012.

[11] J. Colvin, "BGA and Advanced Package Wire to Wire Bonding for Backside Emission Microscopy," *ISTFA 1999 Proceedings,* pp. 365-374, 1999.

[12] J. Colvin, K. Jarausch, "Atomic Force Microscopy: Modes and Analytical Techniques with Scanning Probe Microscopy," *Microelectronics Failure Analysis Desk Reference, 6th edition,* pp. 536-546, 2011.

[13] W. Mack, "3-D System in Package – How to Cope with Increasing Challenges", *EDFA AO (2012)* 3:4-11, pp. 4-11, 2012.

EDFAS
Electronic Device Failure Analysis Society
An Affiliate Society of ASM International

Mr. Jim Colvin
FA Instruments
San Jose, CA

RE: 38th International Symposium for Testing and Failure Analysis
November 11 - 15, 2012
Phoenix Convention Center
Phoenix, AZ, USA

Thank you for your participation at the 38th International Symposium for Testing and Failure Analysis held November 11 - 15, 2012 at the Phoenix Convention Center in Phoenix, AZ, USA. Your presentation, *FemtoFarad/TeraOhm Endpoint Detection for Microsurgery of Integrated Circuit Devices*, was well received at the conference and voted as 2012 Best Paper.

ISTFA's partnership with the International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA) offers the ISTFA 2012 Best Paper winner to attend and present at IPFA 2013. With this, ISTFA will pay for your airfare and IPFA will pay for your hotel and symposium fee.

IPFA 2013 will be July 15 – 19, 2013 in Suzhou, China at the Shangri-La Hotel. For more information regarding IPFA 2013, visit http://ieee-ipfa.org/

You will be contacted in the coming weeks to begin coordinating the details. If you have any questions or need anything at this time, please let me know.

Warm regards,
Jaime Creighton, Event Planner
ASM International