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Robust new process forms 3D shapes from flat sheets of graphene

Researchers from the University of Illinois at Urbana-Champaign have developed a new approach for forming 3D shapes from flat, 2D sheets of graphene, paving the way for future integrated systems of graphene-MEMS hybrid devices and flexible electronics.

"To the best of our knowledge, this study is the first to demonstrate graphene integration to a variety of different microstructured geometries, including pyramids, pillars, domes, inverted pyramids, and the 3D integration of gold nanoparticles (AuNPs)/graphene hybrid structures," explained SungWoo Nam, an assistant professor of mechanical science and engineering at Illinois.

"The flexibility and 3D nature of our structures will enable intimate biosensing devices which can be conformed to the shape and characteristics of human skin and other biological systems. The 3D protruding micro-structures can also achieve enhanced sensitivity by maximizing the effective contact area between the sensors and non-flat surfaces. We also expect that our new 3D integration approach will facilitate advanced classes of hybrid devices between microelectromechanical systems (MEMS) and 2D materials for sensing and actuation."

Graphene, a two-dimensional honeycomb lattice of sp2-bonded carbon atoms, has been widely studied due to its high carrier mobility, chemical inertness, and biocompatibility. To date, various reported methods of graphene transfer have been mostly limited to planar or curvilinear

surfaces due to the challenges associated with fractures from local stress during transfer onto 3D microstructured surfaces. "Our method utilizes wet-transfer and adaptive substrate-engineering, providing several key advantages over other fabrication/integration methods of 3D graphene," stated Jonghyun Choi, a graduate student in Nam's research group and first author of the article, "Three-Dimensional Integration of Graphene via Swelling, Shrinking, and Adaptation," appearing in Nano Letters. "Our results demonstrate a simple, versatile, and scalable method to integrate graphene with 3D geometries with various morphologies and dimensions. Not only are these 3D features larger than those reported in previous works, but we also demonstrate the uniformity and damage-free nature of integrated graphene around the 3D features."

The researchers' robust approach to integrate graphene onto 3D microstructured surfaces maintains the structural integrity of graphene, where the out-of-plane dimensions of the 3D features vary from 3.5 to 50 μm. The process incorporates three sequential steps: 1.) substrate swelling using a solvent that 2.) shrinks during the evaporation process, allowing graphene to 3.) adapt, or conform to the shape of a prepared substrate, to achieve damage-free, large area integration of graphene on 3D microstructures. "Our swelling, shrinking, and adaptation steps are optimized to minimize the degree of graphene suspension around the 3D microstructures and facilitate successful 3D integration," Nam added. "We control the amount of substrate swelling by adjusting the time of immersion in organic solvent and the mixing ratios of monomer and curing agent of the polydimethylsiloxane (PDMS) substrate."

Detailed scanning electron microscopy, atomic force microscopy, Raman spectroscopy, and electrical resistance measurement studies show that the amount of substrate swelling, as well as the flexural rigidities of the transfer film, affect the integration yield and quality of the integrated graphene. To demonstrate the versatility of their approach, the researchers applied the process to a variety of 3D microstructured geometries, as well as integrating hybrid structures of graphene decorated with gold nanoparticles onto 3D microstructure substrates, demonstrating the compatibility of the integration method with other hybrid nanomaterials.

In addition to Nam and Choi, the article's co-authors include Hoe Joon Kim, Michael Cai Wang, Juyoung Leem, and Professor William P. King,

from the Department of Mechanical Science and Engineering at Illinois.
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Source: University of Illinois

First flexible phase-change random access memory

Phase change random access memory (PRAM) is one of the strongest candidates for next-generation non-volatile memory for flexible and wearable electronics. In order to be used as a core memory for flexible devices, the most important issue is reducing high operating current. The effective solution is to decrease cell size in sub-micron region as in commercialized conventional PRAM.

However, the scaling to nano-dimension on flexible substrates is extremely difficult due to soft nature and photolithographic limits on plastics, thus practical flexible PRAM has not been realized yet. Recently, a team led by Professors Keon Jae Lee and Yeon Sik Jung of the Department of Materials Science and Engineering at KAIST has developed the first flexible PRAM enabled by self-assembled block copolymer (BCP) silica nanostructures with an ultralow current operation (below one quarter of conventional PRAM without BCP) on plastic substrates.

BCP is the mixture of two different polymer materials, which can easily create self-ordered arrays of sub-20 nm features through simple spin-coating and plasma treatments. BCP silica nanostructures successfully lowered the contact area by localizing the volume change of phase-change materials and thus resulted in significant power reduction. Furthermore, the ultrathin silicon-based diodes were integrated with phase-change memories (PCM) to suppress the inter-cell interference, which demonstrated random access capability for flexible and wearable electronics. Their work was published in the March issue of ACS Nano:

"Flexible One Diode-One Phase Change Memory Array Enabled by Block Copolymer Self-Assembly."

Another way to achieve ultralow-powered PRAM is to utilize self-structured conductive filaments (CF) instead of the resistor-type conventional heater. The self-structured CF nanoheater originated from unipolar memristor can generate strong heat toward phase-change materials due to high current density through the nanofilament. This ground-breaking methodology shows that sub-10 nm filament heater, without using expensive and non-compatible nanolithography, achieved nanoscale switching volume of phase change materials, resulted in the PCM writing current of below 20 uA, the lowest value among top-down PCM devices.

This achievement was published in the June online issue of ACS Nano: "Self-Structured Conductive Filament Nanoheater for Chalcogenide Phase Transition." In addition, due to self-structured low-power technology compatible to plastics, the research team has recently succeeded in fabricating a flexible PRAM on wearable substrates.

Professor Lee said, "The demonstration of low power PRAM on plastics is one of the most important issues for next-generation wearable and flexible non-volatile memory. Our innovative and simple methodology represents the strong potential for commercializing flexible PRAM." In addition, he wrote a review paper regarding the nanotechnology-based electronic devices in the June online issue of Advanced Materials entitled "Performance Enhancement of Electronic and Energy Devices via Block Copolymer Self-Assembly."

Source: KAIST